IN THE CLAIMS:

Kindly cancel claims 1-87.

Kindly add claims 88-198, as follows:

88. (New) A semiconductor integrated circuit device, wherein the semiconductor integrated circuit device includes a substrate and a plurality of memory cells, and wherein each of the plurality of memory cell comprises:

a transistor, wherein the transistor includes a gate;

a gate oxide, wherein the gate oxide is arranged between the gate and the substrate;

a cell plate, wherein the cell plate is separated from the gate by a predetermined distance, and

wherein a portion of the cell plate overlaps a portion of the gate; and

a dielectric material arranged between the cell plate, the gate and the substrate.

89. (New) The semiconductor integrated circuit device of claim 88, wherein the gate comprises polysilicon.

90. (New) The semiconductor integrated circuit device of claim 88, wherein the cell plate comprises one of polysilicon and a metal conductor.

91. (New) The semiconductor integrated circuit device of claim 88, wherein the dielectric material comprises a high dielectric constant.

92. (New) The semiconductor integrated circuit device of claim 91, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

93. (New) The semiconductor integrated circuit device of claim 88, wherein the cell plate and the gate are positioned in different planes.

94. (New) The semiconductor integrated circuit device of claim 88, wherein the gate is substantially coplanar with another portion of the cell plate.

95. (New) The semiconductor integrated circuit device of claim 88, wherein the semiconductor integrated circuit device is manufactured using a logic process.

96. (New) The semiconductor integrated circuit device of claim 88, wherein the semiconductor integrated circuit device is manufactured using a DRAM process.

97. (New) An apparatus for reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate means and a plurality of means for storing data, and wherein each of the plurality of means for storing data comprises:

a transistor means for switching, wherein the transistor means includes a gate means;

a gate insulating means for insulating the gate means from the substrate means;

a cell plate means for providing an electric field, wherein the cell plate means is separated from the gate means by a predetermined distance, and

wherein a portion of the cell plate means overlaps a portion of the gate means; and

a dielectric means for separating the cell plate means from the gate means and the substrate means.

98. (New) The apparatus of claim 97, wherein the gate means comprises polysilicon.

99. (New) The apparatus of claim 97, wherein the cell plate means comprises one of polysilicon and a metal conductor.

100. (New) The apparatus of claim 97, wherein the dielectric means comprises a high dielectric constant.

101. (New) The apparatus of claim 100, wherein the dielectric means comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

102. (New) The apparatus of claim 97, wherein the cell plate means and the gate means are positioned in different planes.

103. (New) The apparatus of claim 97, wherein the gate means is substantially coplanar with another portion of the cell plate means.

104. (New) The apparatus of claim 97, wherein the DRAM device is manufactured using a logic process.

105. (New) The apparatus of claim 97, wherein the DRAM device is manufactured using a DRAM process.

106. (New) A method of reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate and a plurality of memory cells, wherein each of the plurality of memory cells includes a transistor, wherein the transistor includes a gate and a cell plate, and wherein the method comprises the steps of:

arranging a gate oxide between the gate and the substrate;

separating the cell plate from the gate by a predetermined distance,

wherein a portion of the cell plate overlaps a portion of the gate; and

arranging a dielectric material between the cell plate, the gate and the substrate.

107. (New) The method of claim 106, wherein the gate comprises polysilicon.

108. (New) The method of claim 106, wherein the cell plate comprises one of polysilicon and a metal conductor.

109. (New) The method of claim 106, wherein the dielectric material comprises a high dielectric constant.

110. (New) The method of claim 109, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

111. (New) The method of claim 106, further comprising the step of:
positioning the cell plate and the gate in different planes.

112. (New) The apparatus of claim 106, further comprising the step of:
positioning the gate substantially coplanar with another portion of the cell plate.

113. (New) The method of claim 106, wherein the DRAM device is manufactured using a logic process.

114. (New) The method of claim 106, wherein the DRAM device is manufactured using a DRAM process.

115. (New) A semiconductor integrated circuit device, wherein the semiconductor integrated circuit device includes a substrate and a plurality of memory cells, and wherein each of the plurality of memory cell comprises:

a transistor, wherein the transistor includes a gate;

a gate oxide, wherein the gate oxide is arranged between the gate and the substrate;

a cell plate, wherein the cell plate is laterally separated from the gate by a predetermined distance; and

a dielectric material arranged between the cell plate and the gate and between the cell plate and the substrate.

116. (New) The semiconductor integrated circuit device of claim 115, wherein the gate comprises polysilicon.

117. (New) The semiconductor integrated circuit device of claim 115, wherein the cell plate comprises one of polysilicon and a metal conductor.

118. (New) The semiconductor integrated circuit device of claim 115, wherein the dielectric material comprises a high dielectric constant.

119. (New) The semiconductor integrated circuit device of claim 118, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

120. (New) The semiconductor integrated circuit device of claim 115, wherein the semiconductor integrated circuit device is manufactured using a logic process.

121. (New) The semiconductor integrated circuit device of claim 115, wherein the semiconductor integrated circuit device is manufactured using a DRAM process.

122. (New) An apparatus for reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate means and a plurality of means for storing data, and wherein each of the plurality of means for storing data comprises:

a transistor means for switching, wherein the transistor means includes a gate means;

a gate insulating means for insulating the gate means from the substrate means;

a cell plate means for providing an electric field, wherein the cell plate means is laterally separated from the gate means by a predetermined distance; and

a dielectric means for separating the cell plate means from the gate means and the cell plate means from the substrate means.

123. (New) The apparatus of claim 122, wherein the gate means comprises polysilicon.

124. (New) The apparatus of claim 122, wherein the cell plate means comprises one of polysilicon and a metal conductor.

125. (New) The apparatus of claim 122, wherein the dielectric means comprises a high dielectric constant.

126. (New) The apparatus of claim 125, wherein the dielectric means comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

127. (New) The apparatus of claim 122, wherein the DRAM device is manufactured using a logic process.

128. (New) The apparatus of claim 122, wherein the DRAM device is manufactured using a DRAM process.

129. (New) A method of reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate and a plurality of memory cells, wherein each of the plurality of memory cells includes a transistor, wherein the transistor includes a gate and a cell plate, and wherein the method comprises the steps of:

arranging a gate oxide between the gate and the substrate;

laterally separating the cell plate from the gate by a predetermined distance; and

arranging a dielectric material between the cell plate and the gate and between the cell plate and the substrate.

130. (New) The method of claim 129, wherein the gate comprises polysilicon.

131. (New) The method of claim 129, wherein the cell plate comprises one of polysilicon and a metal conductor.

132. (New) The method of claim 129, wherein the dielectric material comprises a high dielectric constant.

133. (New) The method of claim 132, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

134. (New) The method of claim 129, wherein the DRAM device is manufactured using a logic process.

135. (New) The method of claim 129, wherein the DRAM device is manufactured using a DRAM process.

136. (New) A semiconductor integrated circuit device, including a dynamic random access memory (DRAM) unit, the DRAM unit comprising:

a plurality of bit line pairs,

wherein each bit line pair includes a first bit line and a second bit line,

wherein the first bit line and the second bit line within each bit line pair are aligned with each other in an end-to-end arrangement,

wherein the first bit lines are arranged substantially parallel and consecutively adjacent to one another,

wherein the second bit lines are arranged substantially parallel and consecutively adjacent to one another;

a plurality of word lines,

wherein each word line is associated with one of the first bit lines and the second bit lines such that a first array is formed by the first bit lines and the associated word lines and a second array is formed by the second bit lines and the associated word lines;

a plurality of memory cells,

wherein each of the plurality of memory cells is associated with every other bit line along each word line; and

a first plurality of multiplexers,

wherein each of the first plurality of multiplexers is in communication with two adjacent bits lines within one of the first and second arrays.

137. (New) The semiconductor integrated circuit device of claim 136, wherein, for each word line, each bit line that is not associated with one of the plurality of memory cells acts as a shield between bit lines that are associated with one of the plurality of memory cells.

138. (New) The semiconductor integrated circuit device of claim 136, wherein the DRAM unit further comprises:

a plurality of sense amplifiers,

wherein each of the plurality of sense amplifiers is in communication with a multiplexer associated with two adjacent first bit lines of the first array and a multiplexer associated with two corresponding adjacent second bit lines of the second array.

139. (New) The semiconductor integrated circuit device of claim 51, wherein the DRAM unit further comprises:

a second plurality of multiplexers in communication with a voltage source input and with two adjacent bit lines within one of the first and second arrays.

140. (New) The semiconductor integrated circuit device of claim 139, wherein the array to which an activated word line belongs acts as a sense array, wherein the array to which the activated word line does not belong acts as a reference array, and wherein the DRAM unit further comprises:

a dummy word line in the first array; and

a dummy word line in the second array,

wherein the DRAM unit is configured to detect signal levels in a common mode by activating the dummy word line in the reference array and detecting a signal level of the activated word line differentially as compared to a signal level of the activated dummy word line.

141. (New) The semiconductor integrated circuit device of claim 136, wherein the DRAM unit further comprises:

a first interconnect layer; and

a second interconnect layer,

wherein each bit line is associated with both the first and second interconnect layers.

142. (New) The semiconductor integrated circuit device of claim 141, wherein the first interconnect layer comprises a first metal layer and the second interconnect layer comprises a second metal layer.

143. (New) The semiconductor integrated circuit device of claim 141, wherein the first interconnect layer comprises a metal layer and the second interconnect layer comprises a polysilicon layer.

144. (New) The semiconductor integrated circuit device of claim 141, wherein the first interconnect layer comprises a polysilicon layer and the second interconnect layer comprises a metal layer.

145. (New) The semiconductor integrated circuit device of claim 136, wherein the DRAM unit is manufactured using a logic process.

146. (New) The semiconductor integrated circuit device of claim 136, wherein the DRAM unit is manufactured using a DRAM process.

147. (New) An apparatus for reducing noise and overall bit line capacitance in a dynamic random access memory (DRAM) device, comprising:

a plurality of pairs of bit line means for conducting electrical signals,

wherein each pair of bit line means includes a first bit line means and a second bit line means,

wherein the first bit line means and the second bit line means within each pair of bit line means are aligned with each other in an end-to-end arrangement,

wherein the first bit line means are arranged substantially parallel and consecutively adjacent to one another,

wherein the second bit line means are arranged substantially parallel and consecutively adjacent to one another;

a plurality of word line means,

wherein each word line means is associated with one of the first bit line means

and the second bit line means such that a first array is formed by the first bit line means and the associated word line means and a second array is formed by the second bit line means and the associated word line means;

a plurality of means for storing data,

wherein each of the plurality of means for storing data is associated with every other bit line means along each word line means; and

a first plurality of means for multiplexing,

wherein each of the first plurality of means for multiplexing is in communication with two adjacent bits line means within one of the first and second arrays.

148. (New) The apparatus of claim 147, wherein, for each word line means, each bit line means that is not associated with one of the plurality of means for storing data acts as a shield between bit line means that are associated with one of the plurality of means for storing data.

149. (New) The apparatus of claim 147, further comprising:

a plurality of means for amplifying,

wherein each of the plurality of means for amplifying is in communication with a means for multiplexing associated with two adjacent first bit line means of the first array and a means for multiplexing associated with two corresponding adjacent second bit line means of the second array.

150. (New) The apparatus of claim 149, further comprising:

a second plurality of means for multiplexing in communication with a voltage source input means and with two adjacent bit line means within one of the first and second arrays.

151. (New) The apparatus of claim 150, wherein the array to which an activated word line means belongs acts as a sense array, wherein the array to which the activated word line means does not belong acts as a reference array, and wherein the apparatus further comprises:

a dummy word line means for conducting electrical signals in the first array;

a dummy word line means for conducting electrical signals in the second array; and

means for detecting signal levels in a common mode by activating the dummy word line means in the reference array and detecting a signal level of the activated word line means differentially as compared to a signal level of the activated dummy word line means.

152. (New) The apparatus of claim 147, further comprising:

a first interconnect layer means; and

a second interconnect layer means,

wherein each bit line means is associated with both the first and second interconnect layer means.

153. (New) The apparatus of claim 152, wherein the first interconnect layer means comprises a first metal layer and the second interconnect layer means comprises a second metal layer.

154. (New) The apparatus of claim 152, wherein the first interconnect layer means comprises a metal layer and the second interconnect layer means comprises a polysilicon layer.

155. (New) The apparatus of claim 152, wherein the first interconnect layer means comprises a polysilicon layer and the second interconnect layer means comprises a metal layer.

156. (New) The apparatus of claim 147, wherein the DRAM device is manufactured using a logic process.

157. (New) The apparatus of claim 147, wherein the DRAM device is manufactured using a DRAM process.

158. (New) A method of reducing noise and overall bit line capacitance in a dynamic random access memory (DRAM) device, the DRAM device including a plurality of

bit line pairs, a plurality of word lines, a plurality of memory cells, and a first plurality of multiplexers, wherein each bit line pair includes a first bit line and a second bit line, the method comprising the steps of:

aligning the first bit line and the second bit line within each bit line pair in an end-to-end arrangement;

arranging the first bit lines substantially parallel and consecutively adjacent to one another;

arranging the second bit lines substantially parallel and consecutively adjacent to one another;

associating each word line with one of the first bit lines and the second bit lines such that a first array is formed by the first bit lines and the associated word lines and a second array is formed by the second bit lines and the associated word lines;

associating each of the plurality of memory cells with every other bit line along each word line; and

bringing each of the first plurality of multiplexers into communication with two adjacent bits lines within one of the first and second arrays.

159. (New) The method of claim 158, wherein, for each word line, each bit line that is not associated with one of the plurality of memory cells acts as a shield between bit lines that are associated with one of the plurality of memory cells.

160. (New) The method of claim 158, wherein the DRAM unit further includes a plurality of sense amplifiers, the method further comprising the step of:

bringing each of the plurality of sense amplifiers into communication with a multiplexer associated with two adjacent first bit lines of the first array and a multiplexer associated with two corresponding adjacent second bit lines of the second array.

161. (New) The method of claim 160, wherein the DRAM device further includes a second plurality of multiplexers, the method further comprising the step of:

bringing the each of the second plurality of multiplexers into communication with a voltage source input and with two adjacent bit lines within one of the first and second arrays.

162. (New) The method of claim 161, wherein the array to which an activated word line belongs acts as a sense array, wherein the array to which the activated word line does not belong acts as a reference array, wherein the DRAM device further includes a dummy word line in the first array and a dummy word line in the second array, the method further comprising the step of:

detecting signal levels in a common mode by activating the dummy word line in the reference array and detecting a signal level of the activated word line differentially as compared to a signal level of the activated dummy word line.

163. (New) The method of claim 158, wherein the DRAM device further includes a first interconnect layer and a second interconnect layer, the method further comprising the step of:

associating each bit line with both the first and second interconnect layers.

164. (New) The method of claim 163, wherein the first interconnect layer comprises a first metal layer and the second interconnect layer comprises a second metal layer.

165. (New) The method of claim 163, wherein the first interconnect layer comprises a metal layer and the second interconnect layer comprises a polysilicon layer.

166. (New) The method of claim 163, wherein the first interconnect layer comprises a polysilicon layer and the second interconnect layer comprises a metal layer.

167. (New) The method of claim 158, wherein the DRAM device is manufactured using a logic process.

168. (New) The method of claim 158, wherein the DRAM device is manufactured using a DRAM process.

169. (New) A semiconductor integrated circuit device, including a dynamic random access memory (DRAM) unit, the DRAM unit comprising:

a plurality of bit line pairs,

wherein each bit line pair includes a first bit line and a second bit line,

wherein the first bit line and the second bit line within each bit line pair are aligned adjacent to each other;

a plurality of word lines,

wherein each word line is associated with the bit lines such that an array is formed by the bit lines and the associated word lines;

a first interconnect layer and a second interconnect layer,

wherein each bit line is associated with both the first and second interconnect layers;

a plurality of memory cells,

wherein each of the plurality of memory cells is associated with every other bit line along each word line; and

a plurality of amplifiers,

wherein each of the plurality of amplifiers is in communication with a first bit line and a second bit line within a bit line pair.

170. (New) The semiconductor integrated circuit device of claim 169, wherein, for each word line, each bit line that is not associated with one of the plurality of memory cells acts as a shield between bit lines that are associated with one of the plurality of memory cells.

171. (New) The semiconductor integrated circuit device of claim 169, wherein the DRAM unit further comprises:

a plurality of multiplexers in communication with a voltage source input and with a first bit line and a second bit line within a bit line pair.

172. (New) The semiconductor integrated circuit device of claim 171, wherein the DRAM unit further comprises:

a dummy word line,

wherein the DRAM unit is configured to detect signal levels in a common mode by activating the dummy word line and detecting a signal level of an activated word line differentially as compared to a signal level of the activated dummy word line.

173. (New) The semiconductor integrated circuit device of claim 172, wherein the first bit line and the second bit line within at least one bit line pair are twisted at at least one point such that half of each bit line is associated with the first interconnect layer and half of each bit line is associated with the second interconnect layer.

174. (New) The semiconductor integrated circuit device of claim 169, wherein the first interconnect layer comprises a first metal layer and the second interconnect layer comprises a second metal layer.

175. (New) The semiconductor integrated circuit device of claim 169, wherein the first interconnect layer comprises a metal layer and the second interconnect layer comprises a polysilicon layer.

176. (New) The semiconductor integrated circuit device of claim 169, wherein the first interconnect layer comprises a polysilicon layer and the second interconnect layer comprises a metal layer.

177. (New) The semiconductor integrated circuit device of claim 169, wherein the DRAM unit is manufactured using a logic process.

178. (New) The semiconductor integrated circuit device of claim 169, wherein the DRAM unit is manufactured using a DRAM process.

179. (New) An apparatus for reducing noise and overall bit line capacitance in a dynamic random access memory (DRAM) device, comprising:

a plurality of pairs of bit line means for conducting electrical signals,

wherein each pair of bit line means includes a first bit line means and a second

bit line means,

wherein the first bit line means and the second bit line means within each pair of bit line means are aligned adjacent to each other;

a plurality of word line means,

wherein each word line means is associated with the bit line means such that an array is formed by the bit line means and the associated word line means;

a first interconnect layer means and a second interconnect layer means,

wherein each bit line means is associated with both the first and second interconnect layer means;

a plurality of means for storing data,

wherein each of the plurality of means for storing data is associated with every other bit line means along each word line means; and

a plurality of means for amplifying,

wherein each of the plurality of means for amplifying is in communication with a first bit line means and a second bit line means within a pair of bit line means.

180. (New) The apparatus of claim 179, wherein, for each word line means, each bit line means that is not associated with one of the plurality of means for storing data acts as a shield between bit line means that are associated with one of the plurality of means for storing data.

181. (New) The apparatus of claim 179, further comprising:

a plurality of means for multiplexing in communication with a voltage source input means and with a first bit line means and a second bit line means within a pair of bit line means.

182. (New) The apparatus of claim 181, wherein the apparatus further comprises:

a dummy word line means for conducting electrical signals; and

means for detecting signal levels in a common mode by activating the dummy word line means and detecting a signal level of an activated word line means differentially as compared to a signal level of the activated dummy word line means.

183. (New) The apparatus of claim 182, wherein the first bit line means and the second bit line means within at least one pair of bit line means are twisted at at least one point such that half of each bit line means is associated with the first interconnect layer means and half of each bit line means is associated with the second interconnect layer means.

184. (New) The apparatus of claim 179, wherein the first interconnect layer means comprises a first metal layer and the second interconnect layer means comprises a second metal layer.

185. (New) The apparatus of claim 179, wherein the first interconnect layer means comprises a metal layer and the second interconnect layer means comprises a polysilicon layer.

186. (New) The apparatus of claim 179, wherein the first interconnect layer means comprises a polysilicon layer and the second interconnect layer means comprises a metal layer.

187. (New) The apparatus of claim 179, wherein the DRAM device is manufactured using a logic process.

188. (New) The apparatus of claim 179, wherein the DRAM device is manufactured using a DRAM process.

189. (New) A method of reducing noise and overall bit line capacitance in a dynamic random access memory (DRAM) device, the DRAM device including a plurality of bit line pairs, a plurality of word lines, a plurality of memory cells, a first interconnect layer and a second interconnect layer, and a plurality of amplifiers, wherein each bit line pair includes a first bit line and a second bit line, the method comprising the steps of:

associating each bit line with both the first and second interconnect layers;

aligning the first bit line and the second bit line within each bit line pair to be adjacent

to each other;

associating each word line with the bit lines such that an array is formed by the bit lines and the associated word lines;

associating each of the plurality of memory cells with every other bit line along each word line; and

bringing each of the plurality of amplifiers into communication with a first bit line and a second bit line within a bit line pair.

190. (New) The method of claim 189, wherein, for each word line, each bit line that is not associated with one of the plurality of memory cells acts as a shield between bit lines that are associated with one of the plurality of memory cells.

191. (New) The method of claim 189, wherein the DRAM device further includes a plurality of multiplexers, the method further comprising the step of:

bringing the each of the plurality of multiplexers into communication with a voltage source input and with a first bit line and a second bit line within a bit line pair.

192. (New) The method of claim 191, wherein the DRAM device further includes a dummy word line, the method further comprising the step of:

detecting signal levels in a common mode by activating the dummy word line and detecting a signal level of an activated word line differentially as compared to a signal level of the activated dummy word line.

193. (New) The method of claim 192, further comprising the step of:

twisting the first bit line and the second bit line within at least one pair of bit lines at at least one point such that half of each bit line is associated with the first interconnect layer and half of each bit line is associated with the second interconnect layer.

194. (New) The method of claim 189, wherein the first interconnect layer comprises a first metal layer and the second interconnect layer comprises a second metal layer.

195. (New) The method of claim 189, wherein the first interconnect layer comprises a metal layer and the second interconnect layer comprises a polysilicon layer.

196. (New) The method of claim 189, wherein the first interconnect layer comprises a polysilicon layer and the second interconnect layer comprises a metal layer.

197. (New) The method of claim 189, wherein the DRAM device is manufactured using a logic process.

198. (New) The method of claim 189, wherein the DRAM device is manufactured using a DRAM process.